forming a second layer of a second material over the first layer, the second material having a second work function; and

removing a portion of the first and second layers;

wherein a stack formed by the first and second layers has a work function that is between the first work function and the second work function; and <a href="mailto:providing-optimal channel doping for a predetermined relationship between">providing optimal channel doping for a predetermined relationship between</a> an on current, I<sub>on</sub>, and an off current, I<sub>off</sub>.

- 2. The method Claim 1, wherein the substrate is a silicon wafer with an insulating layer formed thereon.
- 3. The method of Claim 2, wherein the insulating layer comprises an oxide of silicon.
- 4. The method of Claim 2, wherein the second layer is substantially thicker than the first layer.
- 5. Cancelled.

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10. (Currently amended) A method of tuning the work function of a gate electrode, comprising:

forming a layer of a first conductive material superjacent a gate dielectric; and

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forming a layer of a second conductive material superjacent the first conductive material, wherein the thickness of the first conductive material is greater than a first critical thickness and less than a second critical thickness.

- The method of Claim 10, wherein the first conductive material comprises a 11. material selected from the group consisting of TiN, and TaN.
- The method of Claim 10, wherein the second conductive material comprises 12. a material selected from the group consisting Al, Ti, Ta, Ni, Pd, and Pt.
- (Currently amended) The method of Claim 10, wherein the first conductive 13. material comprises TiN, the second material comprises AI, and wherein said first conductive material has a thickness between 20Å and 100Å. the first critical thickness is approximately 20 angstroms and the second critical thickness is approximatley100 angstroms.

14-17. Cancelled

## Please add new claims:

(New) A method of forming a transistor comprising:

forming a gate electrode on an insulating film formed on a semiconductor substrate, wherein said gate electrode comprises a first material selected from the

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group consisting of titanium nitride and tantalum nitride; and a second material formed on the first material wherein the second material is selected from the group consisting of aluminum (AI), palladium (Pd) and platinum (Pt); and forming a pair of source/drain regions in said semiconductor substrate.

- 28. (New) The method of claim 27 wherein said transistor is a NMOS transistor and wherein said first film is titanium nitride and said second film is aluminum.
- 29. (New) The method of claim 27 wherein said transistor is a PMOS transistor and wherein said second material is palladium (Pd).

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